

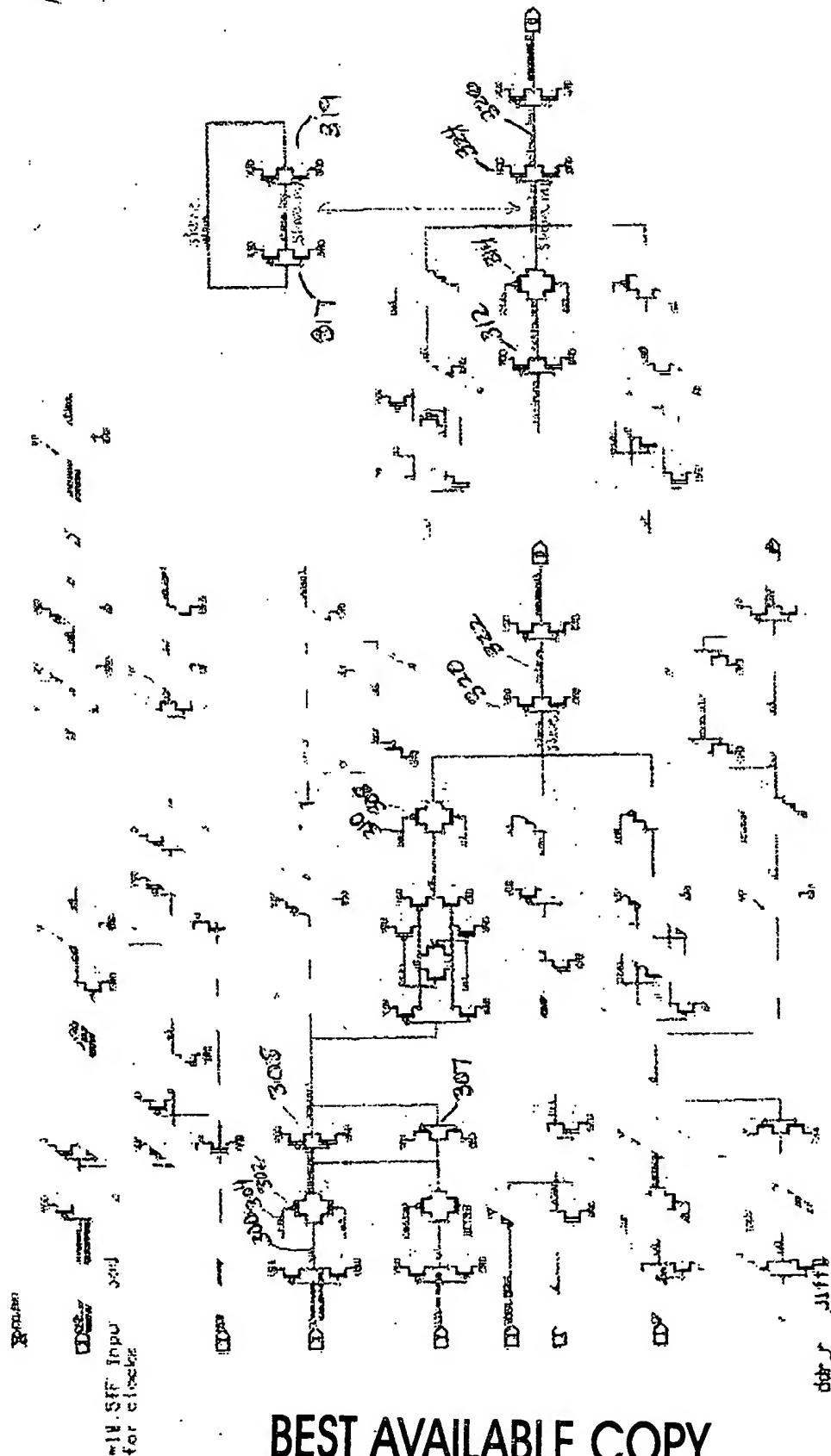
# EXHIBIT A

**WARNING:** This cell is for ddr pads ONLY.  
Use elsewhere at your own risk.

ddr\_req\_diff1 pad ddr register with differential outputs.

**Notes:**  
Assumes non-overlapping complementary clocks.  
Assumes differential master clocks and standard local clock buffers.  
Designed to drive v.ainv.015 load.

To read this schematic, please refer to the notes on the first page of this document.



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